

REMARKS

This is intended as a full and complete response to the Office Action dated September 17, 2007 (hereinafter "the Office Action") having a shortened statutory period for response set to expire on December 17, 2007.

Claims 1-27 were presented for examination. Claims 11-13 have been cancelled without prejudice in order to reduce issues for appeal, should an appeal follow in this prosecution. Claims 1, 8, 14, 24, and 27 have been amended to put the above-captioned application in better condition for appeal, should an appeal follow in this prosecution. Accordingly, claims 1-10 and 14-27 are presently pending.

(1) Real Party in Interest

The above-captioned application is currently owned by Xilinx, Inc., as indicated by an assignment recorded in the Assignment Records of the United States Patent and Trademark Office, details of which shall be provided should an appeal follow in this prosecution.

(2) Related Appeals and Interferences

There are no known prior and pending appeals, interferences, or judicial proceedings known to Applicants, Applicants' legal representative(s), or assignee that may be related to, directly affect or be directly affected by or have a bearing on any decision resulting from an appeal herefrom to the Board of Patent Appeals and Interferences (the "Board").

(3) Status of Claims

Claims 1-27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,487,648 ("Hassoun") in view of U.S. Patent No. 5,625,580 ("Read") and in further view of U.S. Patent No. 5,920,600 ("Yamaoka"). Claims 11-13 have been cancelled without prejudice as indicated above. Accordingly, claims 1-10 and 14-27 presently stand rejected.

(4) Status of Amendments

No amendment(s) have been submitted that were refused entry.

(5) Summary of Claimed Subject Matter

Regarding claims 1, 8, and 14 with reference to the exemplary embodiments as illustratively shown in FIGS. 3A and 3B and FIGS. 4A through 4C, a digital clock module (301) of an integrated circuit (100) is coupled to receive an input clock signal (311). (Specification, at Paragraph [0028].) The input clock signal is used to generate a feedback clock signal (313), and an output clock signal (310) or output clock signals (421-424). (Specification, at Paragraphs [0028] and [0035].) The digital clock module locks onto the feedback clock signal relative to the input clock signal to produce a least common multiple (“LCM”) clock signal (313) and a lock signal (312). (Specification, at Paragraphs [0028], [0030], [0031], and [0036].) The LCM signal and the lock signal are used by a state machine (302, 402, 430) to deassert/assert a control signal (315) for a select circuit or select circuits (305) to mask/unmask the output clock signal or signals for commencing hardware simulation. (Specification, at Paragraphs [0031] through [0034], [0035], [0037], and [0039].)

Regarding claim 27 with reference to the exemplary embodiment as illustratively shown in FIG. 3A and accompanying text (Specification at paragraphs [0027] through [0032]), a test system includes an integrated circuit (100) with a design portion (303) and a first portion of a clock stabilization design portion (306), where the first portion of the clock stabilization design (306) is coupled to a computer (210) that includes a second portion of the clock stabilization design (302). (Specification, Paragraphs [0027] and [0031].) The computer provides an input clock signal (311) to the first portion of the clock stabilization design, and the first portion of the clock stabilization design produces an output clock signal (310), a LCM clock signal (313), and a lock signal (312) for the second portion of the clock stabilization design. (Specification, Paragraphs [0028] and [0031].) The second portion of the clock stabilization design is configured to respond to the lock signal and the LCM clock

signal by asserting a control signal (315) to the first portion of the clock stabilization design indicating sufficient stability of the output clock signal for unmasking or passage thereof to the design portion for initiation of hardware simulation thereof. (Specification, Paragraphs [0031] and [0032].)

Regarding claim 24 with reference to the exemplary embodiment as illustratively shown in FIG. 3B, a test system is similar to that of claim 27, except that the first portion and the second portion of the clock stabilization design are both internal to an the integrated circuit (100) as a clock stabilization design (366). (Specification, Paragraphs [0033] and [0034])

(6) Grounds of Rejection to be Reviewed

Claims 1-10 and 14-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hassoun in view of Read and in further view of Yamaoka.

(7) Argument

The rejection of claims 1-10 and 14-27 under 35 U.S.C. §103(a) is improper and should be withdrawn.

A. Standards of Review

In *ex parte* examination of a patent application, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (MPEP §2142). Only when a *prima facie* case of obviousness is established by the Patent Office does the burden shift to applicant to produce evidence of non-obviousness (MPEP §2142). Accordingly, if the Patent Office does not produce a *prima facie* case of unpatentability, then applicant is entitled to a grant of a patent. *In re Oetiker* 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

One type of *prima facie* case of obviousness requires establishing three basic criteria: (1) some suggestion or motivation either in references themselves or in knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings; (2) a reasonable expectation of

success for the proffered combination; and (3) the prior art reference or references when combined must teach or suggest all the claim limitations. (MPEP §2142). Notably, the teaching or suggestion to make the claim combination and the reasonable expectation of success as set forth in the first two criteria must both be found in the prior art and not based on applicants disclosure. (MPEP §2142, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Recently the Supreme Court clarified application of 35 U.S.C. §103 in *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734, 82 USPQ2d 1385, 1391 (2007) [hereinafter "KSR"]. In that holding the Supreme Court stated that the question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966). In *KSR*, the Supreme Court discussed circumstances in which a patent might be determined to be obvious without an explicit application of the teaching, suggestion, motivation test. *Id.* at 1739, 82 USPQ2d at 1395. The Supreme Court explained:

When a work is available in one field of endeavor, design incentives and other forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 1740, 82 USPQ2d at 1396.

The Supreme Court made it clear that "[f]ollowing these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement." *Id.* The court explained,

“[o]ften, it will be necessary for a court to look to interrelated teaching of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.”

Id. at 1740-41, 82 USPQ2d at 1396.

The Supreme Court noted that “[t]o facilitate review, this analysis should be made explicit.” *Id.* (citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness”). However, “the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *Id.* at 1741, 82 USPQ2d at 1396.

More recently, the Patent Office published Examination Guidelines for Determining Obviousness under 35 U.S.C. §103 in view of the *KSR* holding. While these Examination Guidelines do not constitute substantive rule making, they are intended to be used by the Patent Office personnel to assist them in order “...to make a proper determination of obviousness under 35 U.S.C. 103 and to provide an appropriate supporting rationale.” (72 Fed. Reg. 57526 (October 10, 2007)) In these Examination Guidelines, the underlying inquiries in *Graham* are to be first resolved prior to articulating rationale for such combination. There are several examples of guideline rationales that may be alleged by an Examiner in supporting a conclusion of obviousness.

Thus, presently it appears that there are two guided approaches to an obvious rejection post-*KSR* adopted by the Patent Office. *Id.* at 57528. An obvious rejection may be made using the teaching-suggestion-motivation (“TSM”) rationale, or an obvious rejection may be made using the *KSR* rationale. *Id.*

B. The rejection of claims 1-10 and 14-27 under 35 U.S.C. §103 is improper.

For the reasons set forth below, Applicants respectfully submit that a *prima facie* case of obviousness has not been established by the Patent Office with respect to claims 1-10 and 14-27 as a group.

As indicated by the content of the rejection the Office Action, the *prima facie* case of obviousness being asserted by the Patent Office employs the TSM rationale. As only the TSM rationale is being applied in furtherance of the pending rejection of claims 1-10 and 14-27 under 35 U.S.C. §103, Applicants shall direct the main of their remarks to such TSM rationale of record in the Office Action.

1. No lawful suggestion or motivation to modify.

Applicants respectfully traverse the assertion in the Office Action that it would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the clock detecting system of Yamaoka and the system and method of Read with the device implementation of Hassoun. Specifically, Applicants traverse the assertion in the Office Action that "...it would have been obvious... to combine the clock detecting system of Yamaoka et al. and the system and method of Read et al. with the device implementation of Hassoun because Read et al teaches a reliability and lower cost manufacturing system (col.9 lines 3-5) and further teaches an improvement modeling system (see abstract); and Yamaoka et al. teaches the advantage of achieving high performance easily and at low cost (col.10 lines 22-25)." (Emphasis appears in the original.) (September 17, 2007 Office Action, at: page 5, lines 10-15; page 7, line 20, to page 8, line 3; page 9, lines 9-14; and page 12, lines 17-22). Applicants contend that the cited :"rationale" in the Office Action offers only general motives for combining these particular references.

Even assuming *arguendo* that these objectives of the rationale cited from the Office Action may be met by the combination proffered, Applicants contend

that these general motives do not provide legally sufficient suggestion or motivation for such combination. Again, the Supreme Court noted that “[t]o facilitate review, this analysis should be made explicit.” *KSR* at 1740-41, 82 USPQ2d at 1396. (*citing In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness”).

It is Applicants’ position that the above-cited “conclusory” statements regarding these references provide no “explicit” reasonable basis for the assertion that one of ordinary skill in the art would be led to combine these three particular references out of all the references potentially available. Furthermore, Applicants contend that the references of Hassoun, Read, and Yamaoka are not interrelated, such as were the references in *KSR*. Moreover, Applicants contend that the references of Hassoun, Read, and Yamaoka are so disparate that the only reasonable conclusion is that their combination is improper hindsight reconstruction.

In the Office Action, it is asserted, incorrectly, that Hassoun, Read, and Yamaoka are analogous. Clearly these references are not analogous. Hassoun is for an SDRAM controller for implementation in a PLD. In contrast, Read is for a hardware modeling system. In further contrast, Yamaoka is for bit phase synchronization for high-speed data transmission systems. These references are in three separate fields of endeavor.

Nor are these disparate references directed to the same problem. Hassoun is directed at reducing lead time for development of an SDRAM controller. Read is directed at integrating a hardware modeling system to various simulator platforms, support for ASICs, prototype verification of ASICs, and direct timing measurement of HME output delays. Yamaoka is directed at phase synchronizing incoming transmitted data to a clock of a receiver.

Applicants thus respectfully submit that the only possible basis for combining these references as used in the Office Action is an improper one, namely improper hindsight reconstruction in the light of Applicants' claimed invention.

2. No reasonable expectation of success.

As an initial matter, the Office Action does not even address the issue of a reasonable expectation of success. Given that the burden rests with the Patent Office to demonstrate obviousness, this failure to present evidence for this element of the *prima facie* case suggests that the rejection on the basis of obviousness should be withdrawn.

Applicants are placed in the position of responding to an argument regarding a reasonable expectation of success that has not even been made by the Office Action. In order to ascertain whether there would be such a reasonable expectation of success, there must be some understanding of how the primary reference of Hassoun is to be modified by the secondary references of Read and Yamaoka to arrive at the claimed invention.

Presently, there is no indication in the Office Action of how the teachings of Hassoun are to be reengineered in view of the teachings of Read and Yamaoka to arrive at the claimed invention.

It is Applicant's position that Hassoun is silent as to detecting clock stabilization for hardware simulation. In fact, Hassoun is silent as to hardware simulation at all. What Hassoun discloses is that software is used for creating an SDRAM controller design for instantiation in a PLD. This controller core is provided from the manufacture as a design file. Hassoun goes on to describe this SDRAM controller core, but does not describe whether or how the core is simulated by the manufacture thereof. (*Hassoun*, at col. 7, lines 49-65.)

While Read is not silent with respect to hardware simulation, Read is silent as to detecting clock stabilization as claimed. Read programs an edge to occur

at a time relative to the start of pattern clock. (Read, col. 23, lines 23-63.) Read uses a timing strobe to format pattern data before presenting to the "hardware modeling element" or "HME." (*Id.*) Read is silent with respect to detecting clock stabilization as claimed for providing such strobes. (See, e.g., Read, col. 26, line 9, to col. 27, line 40.)

Again, as both Hassoun and Read are silent as to detecting clock stabilization, there is no basis to provide any indication of how the references may be modified to detect clock stabilization. Furthermore, as indicated below, Yamaoka too is silent as to detecting clock stabilization as claimed.

Applicants respectfully submit that what Yamaoka actually discloses is a phase selector (Yamaoka at FIG. 28) that detects a stable phase timing based on a best phase fit of multiphase (e.g., multiphase clocks 2011-1 through 2011-n) synchronizing to a pattern in a preamble of burst cell data. (Yamaoka, at col. 19, line 3, to col. 21, line 5.) Responsive to establishing synchronization with such a pattern, the data 2017-1 through 2017-3 are output from the phase selector, where data 2017-2 is of the most stable phase, and data 2017-1 and 2017-3 are next to data 2017-2. (*Id.*) Additionally, the phase selector is configured to prevent a selection controller from going into a tracking type synchronization mode until after synchronization has been established by selection of a best phase fit multiphase clock. (*Id.*)

Stability as to synchronization of a clock with a data timing pattern in Yamaoka is not masking an output signal until the output clock signal is sufficiently stabilized as indicated by a control signal for hardware simulation, as claimed in claims 1-10 and 14-26. Furthermore, controlling a transition between a selection type synchronization mode and a tracking type synchronization mode as in Yamaoka is not what is being claimed. Additionally, Yamaoka does not disclose determining stability prior to application of a master clock for selection of a multiphase clock. (E.g., Yamaoka at col. 19, line 67, to col. 20, line 10, makes no mention of first stabilizing a master clock before application thereof.)

Accordingly, it is Applicants' contention that because Yamaoka is silent as to detecting clock stabilization as claimed, its addition to Hassoun and Read, both of which are silent as to detecting clock stabilization, provides no reasonable expectation for success in detecting clock stabilization as claimed.

3. All the claim limitations not taught.

Assuming *arguendo* that modification of Hassoun by Read and Yamaoka is proper, which it is not, Applicants agree with the statements in the Office Action that Hassoun as modified by Read clearly does not teach detecting clock stabilization and masking of an output, as claimed.

According to Hassoun, clock skew and clock delay are addressed using DLLs. (Hassoun, at col. 9, line 58, to col. 10 line 13.) In Hassoun, neither DLL 304A nor DLL 304B produces a lock signal for a state machine. (*Id.*; see also, Hassoun at Figures 3 and 4.) Furthermore, in Hassoun there is no masking of the outputs of DLLs 304A and 304B, as clock outputs from DLLs 304A and 304B are buffered but not masked. (*Id.*)

According to Read, a timing strobe is used to format data before presenting to a hardware modeling element. (Read, col. 23, lines 23-63.) This timing strobe is generated using digital to analog conversion. (Read, col. 26, line 9, to col. 27, line 40.)

In contrast to Hassoun and Read, claims 1-10 and 14-26 each recite in relevant part the features of a lock signal to produce a control signal for masking application of a clock signal. Furthermore, in contrast to Hassoun, claims 24 and 27 each recite in relevant part the features of a lock signal to produce a control signal for selective application of a clock signal.

However, the addition of Yamaoka to Hassoun and Read further does not teach detecting clock stabilization and masking of an output, because in Yamaoka an input clock is decoupled from providing an output clock during a synchronization mode. Applicants respectfully submit that what Yamaoka

discloses is a stable phase selector that detects a stable phase timing based on a best phase fit of a multiphase clock to a pattern in a preamble of burst cell data in a synchronization mode which is decoupled from an input clock. (Yamaoka, at col. 19, line 3, to col. 21, line 5.)

Detector 163 in FIG. 28 of Yamaoka is for matching a preamble PR of a burst data cell. (Yamaoka, at col. 20, lines 11-22.) This synchronization is done using a multiphase clock 2011 from reset VCO 4A input to stable phase selector 16. (Yamaoka at col. 19, lines 11-26.) A reset signal 17 is used to cause the stable phase selector 16 to disable selection controller 6C. (Yamaoka, at col. 19, lines 55-63.) Accordingly, phase control input 2009 to reset VCO 4A is disabled, and VCO 4A runs at a frequency responsive to a frequency control voltage 2003. (e.g., Yamaoka, at col. 5, lines 22-37, with reference to col. 19, lines 27-36.) Furthermore, it should be appreciated that input frequency control voltage 2003 is separate from input clock 2011. In short, output of multiphase clocks 2011 by reset VCO 4A when in a synchronization mode is decoupled from input clock 2011.

In contrast to Yamaoka, all of claims 1-10 and 14-27 recite an input clock used to provide an output clock, the latter of which is masked for clock stabilization. Notably, it stands to reason that if an input clock of Yamaoka is not stable, obtaining synchronization by use of multiphase clocks unrelated to such input clock does not achieve clock stabilization as claimed. Accordingly, even if the proffered combination of Hassoun, Read, and Yamaoka was proper, which it is not, such combination would not teach all of the claimed features.

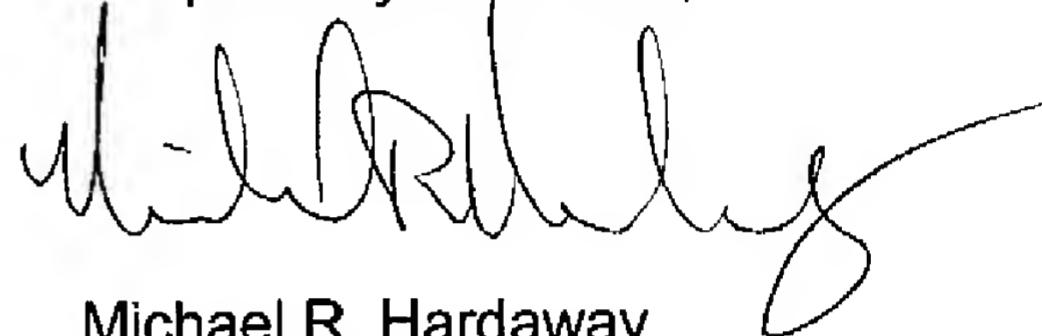
For the above mentioned reasons, Applicants respectfully submit that claims 1-10 and 14-27 should be allowed.

CONCLUSION

All claims should now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-6149.

Respectfully submitted,



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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on December 6, 2007.

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